

**Amendments to the Drawings:**

Applicant submit a new sheet comprising Figures 6A and 6B. No new matter is added.

Attachment: New Sheet

## **REMARKS**

Receipt of the Office action of March 1, 2006 is hereby acknowledged. In that action the Examiner: 1) rejected claims 1-4, 7-10, 24-25 and 30 as allegedly anticipated by McGrath (U.S. Pat. No. 6,560,694); 2) rejected claims 5, 11-12, 14-15, 19, 26 and 29 as allegedly unpatentable over McGrath; 3) rejected claims 6, 13, 16-18, 20-23, and 27-28 as allegedly unpatentable over McGrath in view of Park (U.S. Pat. No. 6,832,305); 4) objected to the drawings; and 5) objected to the specification.

With this Response, Applicant amends claims 6, 9 and 24. Applicant believes the pending claims are allowable over the art of record and respectfully request reconsideration.

### **I. AMENDMENTS TO THE SPECIFICATION**

With respect to paragraphs [0001], [0024], [0027] and [0028], Applicants present a plurality of amendments to add serial numbers and/or patent numbers of related cases, and to correct grammatical shortcomings. Applicants also add paragraphs to address the drawing objections, discussed immediately below. No new matter is added.

### **II. DRAWING OBJECTIONS**

The Office action objects to the drawings for various informalities. To address these concerns, Applicants present Figures 6A and 6B, as well as corresponding paragraphs [0011.1], [0011.2], [0031.1] and [0031.2]. As for Figure 6A and paragraph [0031.1], the figure and paragraph find support in the original disclosure at claims 6, 13, 20 and 28, as well as the original specification paragraphs [0026] and [0029]. As for Figure 6B and paragraph [0031.2], the figure and paragraph find support in the original disclosure at claims 14 and 29, as well as the original specification paragraph [0029]. No new matter is added.

### **III. ART-BASED REJECTIONS**

#### **A. Claim 1**

Claim 1 stands rejected as allegedly anticipated by McGrath.

McGrath is directed to double prefix overrides to provide 16-bit operating size in a 32/64 operating mode. (McGrath Title). In particular, McGrath appears to disclose a processor that can execute programs that take advantage of virtual and physical

address space greater than 32 bits, and can also execute programs that use only 16 bit address space or 32 bit address space.

[T]he compatibility modes supported ... may allow for a 64 bit operating system (i.e. an operating system designed to take advantage of the virtual and physical address spaces in excess of 32 bits and/or data operands of 64 bits) to operate with a 32 bit application program (i.e. an application program written using 32 bit operand and address sizes). ... Furthermore, the operating system may launch a 32 bit application program by establishing one or more 32 bit compatibility mode segment descriptors ... in the segment descriptor table and branching into one of the compatibility mode segments. Similarly, the operating system may launch a 16 bit application program by establishing one or more 16 bit compatibility mode segment descriptors ... in the segment descriptor table and branching into one of the compatibility mode segments. Accordingly, a 64 bit operating system may retain the ability to execute existing 32 bit and 16 bit application programs in the compatibility mode.

(McGrath Col. 8, lines 26-56). McGrath's memory management unit (MMU) 20 sets the address space operating mode of the core 14 based on values in control registers, and a particular address space operating mode can be overridden on a per instruction basis.

MMU 20 generates the operating mode responsive to a code segment descriptor corresponding to the code being executed and further responsive to one or more values in control registers. ... The default operand size may be 32 bits in 32/64 mode, but instructions may override the default 32 bit operand size with a 64 bit operand size when desired.

(McGrath Col. 4, lines 5-18). Thus, the concern of McGrath appears to what type of addressing to use for a particular instruction, and how many bits of operand for an instruction to fetch.

[T]he operating mode may specify a default operand size and a default address size. The default operand size specifies **the number of bits in an operand of an instruction**, unless an instruction's encoding overrides the default. The default address size specifies **the number of bits in an address of a memory operand of an instruction**, unless an instruction's encoding overrides the default. The default address size specifies the size of at least the virtual address of memory operands, and may also specify the size of the physical address.

(McGrath Col. 3, lines 20-29 (emphasis added)).

Claim 1, by contrast, specifically recites a processor comprising “decode logic adapted to decode system commands and instructions in a first mode and in a second mode, wherein the first mode corresponds to a first instruction set and the second mode corresponds to a second instruction set.” Applicants respectfully submit that McGrath does not expressly or inherently teach such a system. McGrath is concerned with the size of the address space and the size of operands to fetch for instructions. McGrath is silent as to the instruction set used. Thus, McGrath does not expressly or inherently teach a processor having a “first mode [that] corresponds to a first instruction set and the second mode [that] corresponds to a second instruction set.” To the extent there is an inherent teaching in McGrath, the inherent teaching would be that the single instruction set used by McGrath is backward compatible to the 32 and 16 bit application programs, not that multiple instruction sets should be supported. For this reason alone the rejection should be withdrawn.

Moreover, claim 1 recites, “and wherein the system commands are accessible in either mode through a common Bytecode.” Even if hypothetically McGrath could be construed to teach two instruction sets (which Applicants do not admit), McGrath still fails to expressly or inherently teach a system where “system commands are accessible in either mode” (*i.e.*, in either instruction set) “through a common Bytecode.”

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend from claim 1 (claims 2-8), should be allowed.

**B. Claim 9**

Claim 9 stands rejected as allegedly anticipated by McGrath. Applicants amend claim 9 to more clearly define over McGrath’s SYSCALL instructions. The amendment finds support in the original specification at Paragraph [0029].

McGrath is directed to double prefix overrides to provide 16-bit operating size in a 32/64 operating mode. (McGrath Title). In particular, McGrath appears to disclose a processor that can execute programs that take advantage of virtual and physical address space greater than 32 bits, and can also execute programs that use only 16 bit address space or 32 bit address space. (McGrath Col. 8, lines 26-56). McGrath’s memory management unit (MMU) 20 sets the address space operating mode of the

core 14 based on values in control registers, and a particular address space operating mode can be overridden on a per instruction basis. (McGrath Col. 4, lines 5-18). Thus, the concern of McGrath appears to what type of addressing to use for a particular instruction, and how many bits of operand for an instruction to fetch. (McGrath Col. 3, lines 20-29).

Claim 9, by contrast, specifically recites "decoding instructions from one instruction set in a current mode; detecting a predetermined prefix indicating a succeeding instruction is a system command; refraining from decoding the predetermined prefix; and decoding the system command when executing instruction in the current mode." Applicants respectfully submit that McGrath does not expressly or inherently teach such a system. The Office action relies on McGrath's SYSCALL instruction for the claimed predetermined prefix. The reliance is misplaced. The SYSCALL routine is clearly decoded and executed, as it is the function which calls a particular operating system routine.

Another method may be the SYSCALL **instruction** supported by processor 10, **which uses a model specific register as the source of the address of the operating system routine.** Updating the model specific registers is a privileged operation, and thus only code executing at a higher privilege level (e.g. operating system code) may establish the address in the model specific register **used by the SYSCALL instruction.**

(McGrath Col. 9, lines 37-43 (emphasis added)). Thus, McGrath's SYSCALL instruction fails to expressly or inherently teach "decoding instructions from one instruction set in a current mode; detecting a predetermined prefix indicating a succeeding instruction is a system command; refraining from decoding the predetermined prefix; and decoding the system command when executing instruction in the current mode."

Based on the foregoing, Applicants respectfully submit that claim 9, and all claims which depend from claim 9 (claims 10-15), should be allowed.

### **C. Claim 16**

Claim 16 stands rejected as allegedly obvious over McGrath and Park.

McGrath is directed to double prefix overrides to provide 16-bit operating size in a 32/64 operating mode. (McGrath Title). In particular, McGrath appears to disclose a

processor that can execute programs that take advantage of virtual and physical address space greater than 32 bits, and can also execute programs that use only 16 bit address space or 32 bit address space. (McGrath Col. 8, lines 26-56). McGrath's memory management unit (MMU) 20 sets the address space operating mode of the core 14 based on values in control registers, and a particular address space operating mode can be overridden on a per instruction basis. (McGrath Col. 4, lines 5-18). Thus, the concern of McGrath appears to what type of addressing to use for a particular instruction, and how many bits of operand for an instruction to fetch. (McGrath Col. 3, lines 20-29). Park is directed to a method and apparatus for executing coprocessor instructions. (Park Title).

Claim 16, by contrast, specifically recites, "decode logic adapted to decode instructions from a first instruction set in a first mode and decode instructions from a second instruction set in a second mode." McGrath fails to teach or fairly suggested a processor utilizing multiple instruction sets, and thus even if the teachings of Park are precisely as the Office action suggests (which Applicants do not admit), McGrath and Park still fail to teach or suggest a "decode logic adapted to decode instructions from a first instruction set in a first mode and decode instructions from a second instruction set in a second mode." For this reason alone the rejection should be withdrawn.

Moreover, claim 16 further recites, "wherein while the decode logic is decoding an instruction from the first instruction set or a second instruction set, the pre-decode logic detects a predetermined prefix indicating a succeeding instruction is a system command, the decode logic remains in a current mode and decodes the succeeding instruction." The Office action relies on McGrath's SYSCALL instruction for the claimed predetermined prefix. The reliance is misplaced. The SYSCALL routine is clearly decoded and executed, as it is the function which calls a particular operating system routine. (McGrath Col. 9, lines 37-43). Thus, even if Park's teachings are precisely as the Office action suggests (again which Applicants do not admit), McGrath's SYSCALL instruction and Park fail to teach or suggest "wherein while the decode logic is decoding an instruction from the first instruction set or a second instruction set, the pre-decode logic detects a predetermined prefix indicating a succeeding instruction is a system

command, the decode logic remains in a current mode and decodes the succeeding instruction."

Based on the foregoing, Applicants respectfully submit that claim 16, and all claims which depend from claim 16 (claims 17-23), should be allowed.

**D. Claim 24**

Claim 24 stands rejected as allegedly anticipated by McGrath. Applicants amend claim 24 to correct a grammatical shortcoming, and not to define over any cited art. This amendment should not be construed as a narrowing amendment.

Claim 24, by contrast, specifically recites a "decode logic adapted to decode instructions from a first instruction set in a first mode and decode instructions from a second instruction set in a second mode." Applicants respectfully submit that McGrath does not expressly or inherently teach such a system. McGrath is concerned with the size of the address space and the size of operands to fetch for instructions. McGrath is silent as to the instruction set used. Thus, McGrath does not expressly or inherently teach a processor having a "decode logic adapted to decode instructions from a first instruction set in a first mode and decode instructions from a second instruction set in a second mode." To the extent there is an inherent teaching in McGrath, the inherent teaching would be that the single instruction set used by McGrath is backward compatible to the 32 and 16 bit application programs, not that multiple instruction sets should be supported.

Based on the foregoing, Applicants respectfully submit that claim 24, and all claims which depend from claim 24 (claims 25-30), should be allowed.

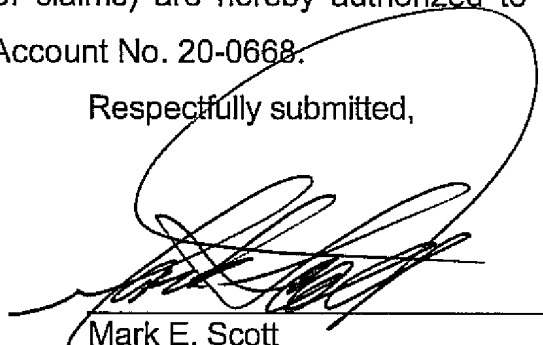
**IV. CONCLUSION**

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between

the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Mark E. Scott', is written over a horizontal line. The signature is stylized with loops and flourishes.

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